TECHNIQUE FOR UTILIZING SPARE BANDWIDTH RESULTING FROM THE USE OF A TRANSITION-LIMITING CODE IN A MULTI-LEVEL SIGNALING SYSTEM

CROSS-REFERENCE TO RELATED APPLICATIONS

5   This patent application is a continuation-in-part application of U.S. Patent Application No. 10/314,985 (Attorney Docket No. 57941.000015; Client Reference No. RA262), filed December 10, 2002, which is hereby incorporated by reference herein in its entirety.

10

FIELD OF THE INVENTION

The present invention relates generally to multi-level signaling and, more particularly, to a technique for utilizing spare bandwidth resulting from the use of a transition-limiting

15   code in a multi-level signaling system.

BACKGROUND OF THE INVENTION

High-speed serial link channels delivering an effective data rate above 5 Gb/s in a backplane environment are subject to

20   significant signal distortion due to inter-symbol interference (ISI). Transmitters and receivers need to compensate for most of the signal distortion using very low complexity schemes in order to obtain a target bit error rate (BER) of less than or equal to 10^{-17} at Gb/s rates and under severe power and

complexity restrictions. This constrained space presents

significant challenges to well-known signal processing and

coding techniques, and sub-optimal but efficient alternatives

are sometimes needed to fulfill the task.

5   Attenuation caused by conductor and dielectric losses

causes dispersion ISI. Another important ISI component is

reflections, which are essentially multipath components of a

signal and originate from impedance discontinuities such as

those caused by connectors of line cards at both transmit and

10   receive ends. In addition to ISI distortion, cross-talk effects

from far and near end adjacent channels is becoming increasingly

significant.

To counteract channel attenuation at high bit rates, 4-

level pulse amplitude modulation (4-PAM) signaling is often used

15   instead of conventional 2-level pulse amplitude modulation (2-

PAM) signaling. That is, in a 2-PAM signaling system, each

conductor in the system may carry signals at one of two signal

levels (i.e., at either a logic zero level or a logic one

level). Thus, in a 2-PAM signaling system, each conductor in

20   the system can only transmit one bit of data per bit time.

However, in a 4-PAM signaling system, each conductor in the

system may carry signals at four different signal levels (i.e.,

four different symbols). Thus, in a 4-PAM signaling system,

each conductor in the system can transmit two bits of data

simultaneously at one half the symbol rate for an equivalent

bandwidth.

In a 4-PAM signaling system that uses current-based output

5   drivers, the four different signal levels are represented by

different current values. For example, the four different

current levels may be identified as 0i, 1i, 2i, and 3i.

Similarly, in a 4-PAM transmission system that uses voltage-

based output drivers, the four different signal levels are

10   represented by different voltage values. For example, the four

different voltage levels may be identified as 0v, 1v, 2v, and

3v. These types of output drivers are typically connected in a

transmission line environment that presents an effective

resistance or impedance to the output driver. This transmission

15   line impedance causes the output voltage to change if the output

current from the current driver changes, and causes the output

current to change if the output voltage from the voltage driver

changes.

A 4-PAM signaling system may be used in systems having

20   either differential pairs of signals or single-ended signals

referenced to ground. In a 4-PAM signaling system utilizing

many single-ended output drivers, it is desirable to maintain

the total signal current required to transmit a byte of data (or

codeword) at a relatively constant current level in comparison to other bytes of data (or codewords). If the signal current fluctuates greatly from one byte to the next, current changes flow through power supply connections and cause noise. These

5 current changes occur when using either voltage drivers or current drivers. The noise on the power supply increases in systems that have high data transmission rates and fast edge rate transmitters. This noise on the power supply degrades the voltage margins of the signals.

10 Understandably, while advantageous in channels with dominant attenuation, 4-PAM signaling systems may be more sensitive to reflections and cross-talk than 2-PAM signaling systems due to the reduction in signal margin as a result of carrying more information per symbol. Thus, in cases where high

15 loss and reflections are combined, the advantages of 4-PAM signaling over 2-PAM signaling may be lost.

In order to preserve the advantages of 4-PAM signaling over 2-PAM signaling, it is desirable to eliminate full-swing transitions (FST) between sequential 4-PAM symbols, as

20 illustrated in the above-referenced U.S. Patent Application No. 10/314,985. This enhances system performance in terms of: 1.) voltage margins (Vm) by reducing peak distortion (PD) via the elimination of one or more worst case sequences; and 2.) timing

margins (Tm), especially at outer eyes where FST close eyes the most.

It is also desirable to secure a minimum density of desirable symbol transitions useful for clock recovery, as also

5 illustrated in the above-referenced U.S. Patent Application No. 10/314,985. These clock data recovery (CDR) transitions prevent continuous phase drifting from an optimum sampling point at the center of an eye in plesiochronous systems with frequency offsets between received data and a local receive clock.

10 As described in the above-referenced U.S. Patent Application No. 10/314,985, transition-limiting codes may be utilized in multi-PAM signaling systems to realize the above-mentioned desirable qualities. As also described in the above-referenced U.S. Patent Application No. 10/314,985, a unique

15 property exists in certain transition-limiting codes, whereby certain outer multi-PAM signal levels are periodically unused. As further described in the above-referenced U.S. Patent Application No. 10/314,985, these periodically unused outer multi-PAM signal levels may be used in framing codewords (i.e.,

20 identifying the boundary of a codeword). However, the use of these periodically unused outer multi-PAM signal levels is not limited in this regard. That is, since these periodically unused outer multi-PAM signal levels essentially constitute

spare bandwidth, it may be desirable to use these periodically

unused outer multi-PAM signal levels for other beneficial

purposes.

In view of the foregoing, it would be desirable to provide

5   a technique for utilizing spare bandwidth resulting from the use

of a transition-limiting code in a multi-level signaling system

in an efficient and cost effective manner.

SUMMARY OF THE INVENTION

10   According to the present invention, a technique for

utilizing spare bandwidth resulting from the use of a

transition-limiting code in a multi-level signaling system is

provided.   In one particular exemplary embodiment, the technique

may be realized as a method for utilizing spare bandwidth

15   resulting from the use of a transition-limiting code in a multi-

level signaling system, wherein the transition-limiting code has

a characteristic wherein a signal level is periodically unused.

Such a method may comprise modifying the transition-limiting

code such that the periodically unused signal level is used to

20   represent additional information.

In accordance with other aspects of this particular

exemplary embodiment of the present invention, the transition-

limiting code may beneficially be formed by encoding digital

values represented by sets of N bits to provide corresponding

sets of P symbols. Also, each set of P symbols may beneficially

be formed with Q bits, wherein Q is greater than N. For

example, N may equal 8 and Q may equal 10, and each symbol may

5   represent two bits.

In accordance with further aspects of this particular

exemplary embodiment of the present invention, modifying the

transition-limiting code may beneficially comprise changing the

logic state of at least one codeword bit in the transition-

10   limiting code.

In accordance with additional aspects of this particular

exemplary embodiment of the present invention, the additional

information may beneficially comprise control information, data

information, error information, framing information, and/or

15   synchronization information.

In accordance with still other aspects of this particular

exemplary embodiment of the present invention, the method may

further beneficially comprise transmitting the modified

transition-limiting code. If such is the case, the modified

20   transition-limiting code may beneficially be transmitted at four

signal levels on a single transmission medium such as, for

example, a single electrical conductor, a differential pair of

electrical conductors, or an optical fiber. Also, the method

may then further beneficially comprise receiving the transmitted

modified transition-limiting code, and detecting the additional

information in the received modified transition-limiting code.

The method may then still further beneficially comprise removing

5   the additional information from the received modified

transition-limiting code so as to return the modified

transition-limiting code to an original unmodified state. The

method may then even still further beneficially comprise

decoding the original transition-limiting code after the

10   additional information is removed.

In accordance with still further aspects of this particular

exemplary embodiment of the present invention, the transition-

limiting code may beneficially have a further characteristic

wherein a plurality of signal levels may be periodically unused,

15   and wherein one or more of the plurality of periodically unused

signal levels may be restricted from being used to represent

additional information at least at certain times. If such is

the case, and if the modified transition-limiting code is

transmitted, the method may further beneficially comprise

20   receiving the transmitted modified transition-limiting code, and

detecting the use of a signal level that has been restricted.

Also, if such is the case, the method may further beneficially

comprise generating an error signal based at least in part upon

the detected restricted signal level use.

In another particular exemplary embodiment of the present invention, the technique may be realized as at least one signal embodied in at least one carrier wave for transmitting a

5 computer program of instructions configured to be readable by at least one processor for instructing the at least one processor to execute a computer process for performing the above-described method.

In still another particular exemplary embodiment of the

10 present invention, the technique may be realized as at least one processor readable carrier for storing a computer program of instructions configured to be readable by at least one processor for instructing the at least one processor to execute a computer process for performing the above-described method.

15 In still another particular exemplary embodiment of the present invention, the technique may be realized as an apparatus for utilizing spare bandwidth resulting from the use of a transition-limiting code in a multi-level signaling system, wherein the transition-limiting code has a characteristic

20 wherein a signal level is periodically unused. Such an apparatus may comprise a modifier for modifying the transition-limiting code such that the periodically unused signal level is used to represent additional information.

In accordance with other aspects of this particular exemplary embodiment of the present invention, the apparatus may further beneficially comprise a transmitter for transmitting the modified transition-limiting code, a receiver for receiving the

5 transmitted modified transition-limiting code, a detector for detecting the additional information in the received modified transition-limiting code, and/or a decoder for decoding the original transition-limiting code after the additional information is removed.

10 In accordance with further aspects of this particular exemplary embodiment of the present invention, the transition-limiting code may beneficially have a further characteristic wherein a plurality of signal levels may be periodically unused, and wherein one or more of the plurality of periodically unused

15 signal levels may be restricted from being used to represent additional information at least at certain times. If such is the case, and if the modified transition-limiting code is transmitted, the apparatus may further beneficially comprise a receiver for receiving the transmitted modified transition-

20 limiting code, and a detector for detecting the use of a signal level that has been restricted. Also, if such is the case, the detector may beneficially generate an error signal based at least in part upon the detected restricted signal level use.

In accordance with additional aspects of this particular exemplary embodiment of the present invention, the apparatus may beneficially comprise additional features similar to those recited above with respect to the above-described method.

5   The present invention will now be described in more detail with reference to exemplary embodiments thereof as shown in the accompanying drawings. While the present invention is described below with reference to exemplary embodiments, it should be understood that the present invention is not limited thereto.

10   Those of ordinary skill in the art having access to the teachings herein will recognize additional implementations, modifications, and embodiments, as well as other fields of use, which are within the scope of the present invention as disclosed and claimed herein, and with respect to which the present

15   invention could be of significant utility.

BRIEF DESCRIPTION OF THE DRAWINGS

In order to facilitate a fuller understanding of the present invention, reference is now made to the accompanying

20   drawings, in which like elements are referenced with like numerals. These drawings should not be construed as limiting the present invention, but are intended to be exemplary only.

Figure 1 shows a signal transition diagram for a 4-PAM

signaling system utilizing a 4S5S transition-limiting code.

Figure 2 shows a plurality of state transition diagrams for a 4-PAM signaling system utilizing a 4S5S transition-limiting code.

5   Figure 3 shows a generic 4-PAM signaling system for supporting a technique for utilizing spare bandwidth resulting from the use of transition-limiting codes in accordance with one embodiment of the present invention.

Figure 4 shows symbol domain and codeword bit domain logic

10   tables for determining when spare bandwidth associated with periodically unused outer 4-PAM signal levels may be used for other beneficial purposes in a first scenario in accordance with one embodiment of the present invention.

Figure 5 shows symbol domain and codeword bit domain logic

15   tables for determining when spare bandwidth associated with periodically unused outer 4-PAM signal levels may be used for other beneficial purposes in a second scenario in accordance with one embodiment of the present invention.

Figure 6 shows symbol domain and codeword bit domain logic

20   tables for determining when spare bandwidth associated with periodically unused outer 4-PAM signal levels may be used for other beneficial purposes in a third scenario in accordance with one embodiment of the present invention.

Figures 7A and 7B show modified 4S5S encoder circuitry for use in utilizing spare bandwidth resulting from the use of a 4S5S transition-limiting code in a 4-PAM signaling system in accordance with embodiments of the present invention.

5   Figures 8A and 8B show modified 4S5S encoder and serializing 4-PAM transmitter circuitry for use in utilizing spare bandwidth resulting from the use of a 4S5S transition-limiting code in a 4-PAM signaling system in accordance with embodiments of the present invention.

10   Figures 9A and 9B show circuitry for use in receiving and decoding codewords that have been modified to utilize spare bandwidth resulting from the use of a 4S5S transition-limiting code in a 4-PAM signaling system in accordance with embodiments of the present invention.

15   Figures 10A and 10B show alternative circuitry for use in receiving and decoding codewords that have been modified to utilize spare bandwidth resulting from the use of a 4S5S transition-limiting code in a 4-PAM signaling system in accordance with embodiments of the present invention.

20   Figure 11 shows symbol domain and codeword bit domain logic tables for determining when spare bandwidth associated with periodically unused outer 4-PAM signal levels may be used for error detection in accordance with one embodiment of the present

invention.

Figures 12A and 12B show circuitry for use in receiving and decoding codewords that may have been modified to utilize spare bandwidth resulting from the use of a 4S5S transition-limiting

5   code in a 4-PAM signaling system in accordance with embodiments of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENT(S)

Referring to Figure 1, there is shown a signal transition

10   diagram for a 4-PAM signaling system utilizing a 4S5S transition-limiting code as described in the above-referenced U.S. Patent Application No. 10/314,985. As shown in Figure 1, the 4S5S transition-limiting code has a unique property wherein two outer 4-PAM signal levels are periodically unused. That is,

15   assuming T is a symbol period, every 5T two outer 4-PAM signal levels (i.e., the uppermost and lowermost signal levels) are not used (i.e., there are no transitions starting from or ending at two outer 4-PAM signal levels). As described in the above-referenced U.S. Patent Application No. 10/314,985, these

20   periodically unused outer 4-PAM signal levels may be used in framing codewords (i.e., identifying the boundary of a codeword). However, the use of these periodically unused outer 4-PAM signal levels is not limited in this regard. That is,

since these periodically unused outer 4-PAM signal levels

essentially constitute spare bandwidth, these periodically

unused outer 4-PAM signal levels may be used for other

beneficial purposes in accordance with the present invention.

5   Referring to Figure 2, there is shown a plurality of state

transition diagrams for a 4-PAM signaling system utilizing a

4S5S transition-limiting code as described in the above-

referenced U.S. Patent Application No. 10/314,985. In the 4S5S

transition-limiting code described in the above-referenced U.S.

10   Patent Application No. 10/314,985, the outer 4-PAM signal levels

are periodically unused. One reason for periodically not using

the outer 4-PAM signal levels is to eliminate full-swing

transitions between symbols. Eliminating full-swing transitions

can reduce signal distortions, such as inter-symbol interference

15   (ISI), which can affect speed and/or the error rate at which

data can be transmitted.

The plurality of state transition diagrams shown in Figure

2 illustrate four separate cases (i.e., Cases I, II, III, and

IV) when the above-described periodically unused outer 4-PAM

20   signal levels may or may not be used for other beneficial

purposes in accordance with the present invention. In each

case, a symbol may be represented by $s_x^{(k)}$, wherein x represents

the symbol number within a codeword, and k represents the

codeword number. In the embodiment described with respect to Figure 2, the periodically unused outer 4-PAM signals levels are located in the 1st symbol of each codeword (i.e., at each $s_1^{(k+1)}$ signal level). For example, in Case I, when the signal level of

5 the fifth symbol in a first codeword (i.e., $s_5^{(k)}$, wherein k = 1, 2, 3,...) is 00 and the signal level of the second symbol in a second codeword (i.e., $s_2^{(k+1)}$, wherein k = 1, 2, 3,...) is 00, 01, or 11, then the uppermost signal level (i.e., 00) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1,

10 2, 3,...) may be used for other beneficial purposes in accordance with the present invention. This is because such use would not violate the transition-limiting properties (e.g., elimination of full-swing transitions) of the transition-limiting code. For example, if $s_5^{(k)}$ is 00 and $s_2^{(k+1)}$ is 11, then

15 $s_1^{(k+1)}$ may be 00 because neither the transition from $s_5^{(k)}$ to $s_1^{(k+1)}$ (i.e., 00 to 00) nor the transition from $s_1^{(k+1)}$ to $s_2^{(k+1)}$ (i.e., 00 to 11) is a full-swing transition when using the Gray code assignment shown in Figure 2. Also in Case I, when the signal level of the second symbol in the second codeword (i.e., $s_2^{(k+1)}$,

20 wherein k = 1, 2, 3,...) is 00 and the signal level of the fifth symbol in the first codeword (i.e., $s_5^{(k)}$, wherein k = 1, 2, 3,...) is 01 or 11, then the uppermost signal level (i.e., 00) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein

$k = 1, 2, 3, \ldots$) may be used for other beneficial purposes in accordance with the present invention because such use would not violate the transition-limiting properties of the transition-limiting code. However, the lowermost signal level (i.e., 10)

5 of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein $k = 1, 2, 3, \ldots$) may not be used for other beneficial purposes in accordance with the present invention in any of the above-mentioned Case I scenarios because such use would violate the transition-limiting properties of the transition-limiting code.

10 Analogously, in Case II, when the signal level of the fifth symbol in the first codeword (i.e., $s_5^{(k)}$, wherein $k = 1, 2, 3, \ldots$) is 10 and the signal level of the second symbol in the second codeword (i.e., $s_2^{(k+1)}$, wherein $k = 1, 2, 3, \ldots$) is 01, 11, or 10, then the lowermost signal level (i.e., 10) of the

15 first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein $k = 1, 2, 3, \ldots$) may be used for other beneficial purposes in accordance with the present invention because such use would not violate the transition-limiting properties of the transition-limiting code. Also in Case II, when the signal level of the

20 second symbol in the second codeword (i.e., $s_2^{(k+1)}$, wherein $k = 1, 2, 3, \ldots$) is 10 and the signal level of the fifth symbol in the first codeword (i.e., $s_5^{(k)}$, wherein $k = 1, 2, 3, \ldots$) is 01 or 11, then the lowermost signal level (i.e., 10) of the first

symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) may be used for other beneficial purposes in accordance with the present invention because such use would not violate the transition-limiting properties of the transition-limiting

5   code. However, the uppermost signal level (i.e., 00) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) may not be used for other beneficial purposes in accordance with the present invention in any of the above-mentioned Case II scenarios because such use would violate the

10 transition-limiting properties of the transition-limiting code.

In Case III, when the signal level of the fifth symbol in the first codeword (i.e., $s_5^{(k)}$, wherein k = 1, 2, 3,...) is 10 and the signal level of the second symbol in the second codeword (i.e., $s_2^{(k+1)}$, wherein k = 1, 2, 3,...) is 00, then neither the

15 uppermost signal level (i.e., 00) nor the lowermost signal level (i.e., 10) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) may be used for other beneficial purposes in accordance with the present invention because such use would violate the transition-limiting properties of the

20 transition-limiting code. Also in Case III, when the signal level of the fifth symbol in the first codeword (i.e., $s_5^{(k)}$, wherein k = 1, 2, 3,...) is 00 and the signal level of the second symbol in the second codeword (i.e., $s_2^{(k+1)}$, wherein k =

1, 2, 3,...) is 10, then neither the uppermost signal level

(i.e., 00) nor the lowermost signal level (i.e., 10) of the

first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1,

2, 3,...) may be used for other beneficial purposes in

5   accordance with the present invention because such use would

violate the transition-limiting properties of the transition-

limiting code.

However, in Case IV, when the signal level of the fifth

symbol in the first codeword (i.e., $s_5^{(k)}$, wherein k = 1, 2,

10   3,...) is 01 and the signal level of the second symbol in the

second codeword (i.e., $s_2^{(k+1)}$, wherein k = 1, 2, 3,...) is 01 or

11, then either the uppermost signal level (i.e., 00) or the

lowermost signal level (i.e., 10) of the first symbol in the

second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) may be

15   used for other beneficial purposes in accordance with the

present invention because such use would not violate the

transition-limiting properties of the transition-limiting code.

Also in Case IV, when the signal level of the fifth symbol in

the first codeword (i.e., $s_5^{(k)}$, wherein k = 1, 2, 3,...) is 11

20   and the signal level of the second symbol in the second codeword

(i.e., $s_2^{(k+1)}$, wherein k = 1, 2, 3,...) is 01 or 11, then either

the uppermost signal level (i.e., 00) or the lowermost signal

level (i.e., 10) of the first symbol in the second codeword

(i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) may be used for other beneficial purposes in accordance with the present invention because such use would not violate the transition-limiting properties of the transition-limiting code.

5   At this point it should be noted that the signal level designations shown in Figures 1 and 2 are such that a two-bit binary value is assigned to each signal level (e.g., a Gray code assignment). Each sequential symbol carries this two-bit binary value in a 4-PAM signaling system. It should be noted, however,

10   that the present invention is not limited to 4-PAM signaling systems or to signal level designations having Gray code assignments.

        At this point it should be noted that the binary signal level designations shown in Figures 1 and 2 may be associated

15   with many different combinations of signal voltage, current, or other unit levels. For example, in a very simplified case, the 00 binary signal level designation may be associated with +0.500 volts, the 01 binary signal level designation may be associated with +0.167 volts, the 11 binary signal level designation may be

20   associated with -0.167 volts, and the 10 binary signal level designation may be associated with -0.500 volts. Of course, the present invention is not limited in this regard since, as mentioned above, the binary signal level designations shown in

Figures 1 and 2 may be associated with many different

combinations of signal voltages. The present invention may also

be used in systems in which the signal level designations are

expressed in terms of current, or other unit, levels. In some

5   instances, it is useful to express the binary signal level

designations using unitless values which are representative of

normalized amplitudes of voltages associated with the binary

signal level designations. For example, in a 4-PAM signaling

system, the binary signal level designations may be expressed as

10   -3, -1, +1, and +3. Expressing the binary signal level

designations in this manner facilitates expressing the sum of

the levels and differences between levels as integer values.

It should also be noted that, with respect to Cases I - IV

shown in Figure 2, the primary transition-limiting property of

15   the transition-limiting code was generally the elimination of

full-swing transitions between symbols, and specifically the

elimination of full-swing transitions to/from the first symbol

of each codeword. Other transition-limiting codes using

different transition-limiting properties in addition to, or

20   instead of, the elimination of full-swing transitions may be

used. For example, in order to further reduce signal

distortion, a transition-limiting code having transition-

limiting properties of eliminating both full and second order

swing transitions may be used. In such an example, again using

a Gray code assignment and the symbol definition provided above,

when $s_5^{(k)}$ is 00 and $s_2^{(k+1)}$ is either 00 or 01, then $s_1^{(k+1)}$ may be

00 because neither the transition from $s_5^{(k)}$ to $s_1^{(k+1)}$ (i.e., 00 to

5   00) nor the transitions from $s_1^{(k+1)}$ to $s_2^{(k+1)}$ (i.e., 00 to 00 or 00

to 01) are full or second order swing transitions, and the upper

4-PAM signal level can still be used for other beneficial

purposes. In another example, the transition-limiting

properties of the transition-limiting code may include the

10 elimination of full-swing transitions and a guaranteed clock

data recovery (CDR) transition density. For example, the

guaranteed CDR transition density may require that there be at

least one symbol transition in the 4 possible symbol transitions

in a 5 symbol codeword. In such an example, if $s_2^{(k+1)}$ is 00,

15 $s_3^{(k+1)}$ is 00, $s_4^{(k+1)}$ is 00, and $s_5^{(k+1)}$ is 00, then the CDR

transition density property would prohibit $s_1^{(k+1)}$ from being

changed from 01 to 00.

Referring to Figure 3, there is shown an exemplary

embodiment of a 4-PAM signaling system 100 comprising an encoder

20 102, a serializing 4-PAM transmitter 104, a deserializing 4-PAM

receiver 106, and a decoder 108. The serializing 4-PAM

transmitter 104 and the deserializing 4-PAM receiver 106 are

interconnected by a pair of signal carrying conductors 110.

In the embodiment of Figure 3, the encoder 102 receives parallel input data D_{in}, and then encodes the received parallel input data D_{in} so as to provide parallel codewords to the serializing 4-PAM transmitter 104 that are organized as MSB

5   codewords (M) and LSB codewords (L). The MSB codewords (M) and the LSB codewords (L) together include multiple consecutive symbols. The parallel input data D_{in} is received as a word having x+1 bits. The MSB codewords (M) and the LSB codewords (L) each have y+1 bits. The encoder 102 may be implemented with

10   binary logic, as described in the above-referenced U.S. Patent Application No. 10/314,985.

The serializing 4-PAM transmitter 104 receives the MSB codewords (M) and the LSB codewords (L) in parallel form from the encoder 102. The serializing 4-PAM transmitter 104

15   comprises a differential transmitter 112 for differentially serially transmitting the received multiple consecutive symbols in the MSB codewords (M) and the LSB codewords (L) over the pair of signal carrying conductors 110 to the deserializing 4-PAM receiver 106.

20   The deserializing 4-PAM receiver 106 comprises a differential receiver 114 for differentially serially receiving the multiple consecutive symbols in the MSB codewords (M) and the LSB codewords (L) over the pair of signal carrying

conductors 110 from the serializing 4-PAM transmitter 104. The

differential receiver 114 then transmits the MSB codewords (M)

and the LSB codewords (L) in parallel form to the decoder 108.

The decoder 108 is essentially the inverse of the encoder

5   102. That is, the decoder 108 receives the MSB codewords (M)

and the LSB codewords (L) in parallel form from the

deserializing 4-PAM receiver 106, and then decodes the received

MSB codewords (M) and the received LSB codewords (L) so as to

provide parallel output data D_{out}. The parallel output data D_{out}

10   is provided as a word having x+1 bits. The decoder 108 may be

implemented with binary logic, as described in the above-

referenced U.S. Patent Application No. 10/314,985.

At this point it should be noted that, while Figure 3 shows

the serializing 4-PAM transmitter 104 as having the differential

15   transmitter 112 and the deserializing 4-PAM receiver 106 as

having the differential receiver 114, the present invention is

not limited in this regard. That is, the MSB codewords (M) and

the LSB codewords (L) may be transmitted from the serializing 4-

PAM transmitter 104 to the deserializing 4-PAM receiver 106 in a

20   single-ended manner requiring only a single-ended transmitter

and a single-ended receiver. Thus, the serializing 4-PAM

transmitter 104 and the deserializing 4-PAM receiver 106 may

alternatively be interconnected by a single signal carrying

conductor instead of the pair of signal carrying conductors 110. Alternatively still, in an optical based system, the serializing 4-PAM transmitter 104 and the deserializing 4-PAM receiver 106 may be interconnected by an optical fiber capable carrying

5   signals at multiple optical signal levels. Alternatively even still, in a wireless based system, the serializing 4-PAM transmitter 104 and the deserializing 4-PAM receiver 106 may not be interconnected by any fixed transmission medium, but rather the MSB codewords (M) and the LSB codewords (L) may be

10   transmitted from the serializing 4-PAM transmitter 104 to the deserializing 4-PAM receiver 106 via a wireless protocol.

For purposes of clearly describing the present invention, assume that the 4-PAM signaling system 100 shown in Figure 3 is utilizing a 4S5S transition-limiting code as described in the

15   above-referenced U.S. Patent Application No. 10/314,985. Thus, in the embodiment of Figure 3, the encoder 102 receives parallel input data $D_{in}<7:0>$, and then encodes the received parallel input data $D_{in}<7:0>$ so as to provide parallel codewords to the serializing 4-PAM transmitter 104 that are organized as MSB

20   codewords ($M<4:0>$) and LSB codewords ($L<4:0>$). The parallel input data $D_{in}<7:0>$ is received as an 8-bit word. The MSB codewords ($M<4:0>$) and the LSB codewords ($L<4:0>$) each have 5 bits, wherein each MSB codeword ($M<4:0>$) has five codeword bits

organized as $<C_1, C_3, C_5, C_7, C_9>$ and each LSB codeword (L<4:0>)

has five codeword bits organized as $<C_2, C_4, C_6, C_8, C_{10}>$. Thus,

the MSB codewords (M<4:0>) and the LSB codewords (L<4:0>)

together form 10-bit codewords (i.e., C_1, C_2, C_3, C_4, C_5, C_6, C_7,

5   C_8, C_9, C_{10}) that are represented by groups of consecutive 2-bit

symbols (i.e., C_1 & C_2, C_3 & C_4, C_5 & C_6, C_7 & C_8, and C_9 & C_{10}).

Referring to Figure 4, there are shown symbol domain and

codeword bit domain logic tables for determining when spare

bandwidth associated with periodically unused outer 4-PAM signal

10   levels may be used for other beneficial purposes in the above-

described Case I scenario (see Figure 2) in accordance with the

present invention. That is, if the Case I conditions as defined

in Figure 4 are met, then the uppermost signal level (i.e., 00)

of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein

15   k = 1, 2, 3,...) may be used for other beneficial purposes in

accordance with the present invention.

In the Case I(a) scenario, the use of the uppermost signal

level (i.e., 00) of the first symbol in the second codeword

(i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) comprises utilizing the C_2

20   bit in the LSB codeword (L<4:0>) to represent additional

information. That is, the C_2 bit in the LSB codeword (L<4:0>)

may be changed from a logic "1" state to a logic "0" state,

thereby changing the signal level of the first symbol in the

second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) from a

logic "01" signal level (e.g., represented by +1) to a logic

"00" signal level (e.g., represented by +3). This change in the

logic state of the C_2 bit in the LSB codeword (L<4:0>) may

5   represent any number of types of additional information, such

as, for example, control information, data information, error

information, framing information, synchronization information,

etc..

In the Case I(b) scenario, the use of the uppermost signal

10   level (i.e., 00) of the first symbol in the second codeword

(i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) comprises utilizing the C_1

bit in the MSB codeword (M<4:0>) and the C_2 bit in the LSB

codeword (L<4:0>) to represent additional information. That is,

the C_1 bit in the MSB codeword (M<4:0>) may be changed from a

15   logic "1" state to a logic "0" state and the C_2 bit in the LSB

codeword (L<4:0>) may be changed from a logic "1" state to a

logic "0" state, thereby changing the signal level of the first

symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2,

3,...) from a logic "11" signal level (e.g., represented by -1)

20   to a logic "00" signal level (e.g., represented by +3). This

change in the logic states of the C_1 bit in the MSB codeword

(M<4:0>) and the C_2 bit in the LSB codeword (L<4:0>) may

represent any number of types of additional information, such

as, for example, control information, data information, error

information, framing information, synchronization information,

etc..

Referring to Figure 5, there are shown symbol domain and

5   codeword bit domain logic tables for determining when spare

bandwidth associated with periodically unused outer 4-PAM signal

levels may be used for other beneficial purposes in the above-

described Case II scenario (see Figure 2) in accordance with the

present invention. That is, if the Case II conditions as

10   defined in Figure 5 are met, then the lowermost signal level

(i.e., 10) of the first symbol in the second codeword (i.e.,

$s_1^{(k+1)}$, wherein k = 1, 2, 3,...) may be used for other beneficial

purposes in accordance with the present invention.

In the Case II(a) scenario, the use of the lowermost signal

15   level (i.e., 10) of the first symbol in the second codeword

(i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) comprises utilizing the C_2

bit in the LSB codeword (L<4:0>) to represent additional

information. That is, the C_2 bit in the LSB codeword (L<4:0>)

may be changed from a logic "1" state to a logic "0" state,

20   thereby changing the signal level of the first symbol in the

second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) from a

logic "11" signal level (e.g., represented by -1) to a logic

"10" signal level (e.g., represented by -3). This change in the

logic state of the C_2 bit in the LSB codeword (L<4:0>) may

represent any number of types of additional information, such

as, for example, control information, data information, error

information, framing information, synchronization information,

5   etc..

In the Case II(b) scenario, the use of the lowermost signal

level (i.e., 10) of the first symbol in the second codeword

(i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) comprises utilizing the C_1

bit in the MSB codeword (M<4:0>) and the C_2 bit in the LSB

10 codeword (L<4:0>) to represent additional information. That is,

the C_1 bit in the MSB codeword (M<4:0>) may be changed from a

logic "0" state to a logic "1" state and the C_2 bit in the LSB

codeword (L<4:0>) may be changed from a logic "1" state to a

logic "0" state, thereby changing the signal level of the first

15 symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2,

3,...) from a logic "01" signal level (e.g., represented by 1)

to a logic "10" signal level (e.g., represented by -3). This

change in the logic states of the C_1 bit in the MSB codeword

(M<4:0>) and the C_2 bit in the LSB codeword (L<4:0>) may

20 represent any number of types of additional information, such

as, for example, control information, data information, error

information, framing information, synchronization information,

etc..

Referring to Figure 6, there are shown symbol domain and codeword bit domain logic tables for determining when spare bandwidth associated with periodically unused outer 4-PAM signal levels may be used for other beneficial purposes in the above-

5   described Case IV scenario (see Figure 2) in accordance with the present invention. That is, if the Case IV conditions as defined in Figure 6 are met, then either the uppermost signal level (i.e., 00) or the lowermost signal level (i.e., 10) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1,

10 2, 3,...) may be used for other beneficial purposes in accordance with the present invention.

In the Case IV(a) scenario, the use of the uppermost signal level (i.e., 00) or the lowermost signal level (i.e., 10) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1,

15 2, 3,...) comprises utilizing the C_2 bit in the LSB codeword (L<4:0>) to represent additional information. That is, the C_2 bit in the LSB codeword (L<4:0>) may be changed from a logic "1" state to a logic "0" state, thereby changing the signal level of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k

20 = 1, 2, 3,...) from a logic "01" signal level (e.g., represented by +1) to a logic "00" signal level (e.g., represented by +3). Alternatively, the C_2 bit in the LSB codeword (L<4:0>) may be changed from a logic "1" state to a logic "0" state, thereby

changing the signal level of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) from a logic "11" signal level (e.g., represented by -1) to a logic "10" signal level (e.g., represented by -3). These changes in the

5   logic state of the C_2 bit in the LSB codeword (L<4:0>) may represent any number of types of additional information, such as, for example, control information, data information, error information, framing information, synchronization information, etc..

10   In the Case IV(b) scenario, the use of the uppermost signal level (i.e., 00) or the lowermost signal level (i.e., 10) of the first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) comprises utilizing the C_1 bit in the MSB codeword (M<4:0>) and the C_2 bit in the LSB codeword (L<4:0>) to represent

15   additional information. That is, the C_1 bit in the MSB codeword (M<4:0>) may be changed from a logic "1" state to a logic "0" state and the C_2 bit in the LSB codeword (L<4:0>) may be changed from a logic "1" state to a logic "0" state, thereby changing the signal level of the first symbol in the second codeword

20   (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) from a logic "11" signal level (e.g., represented by -1) to a logic "00" signal level (e.g., represented by +3). Alternatively, the C_1 bit in the MSB codeword (M<4:0>) may be changed from a logic "0" state to a

logic "1" state and the C_2 bit in the LSB codeword (L<4:0>) may

be changed from a logic "1" state to a logic "0" state, thereby

changing the signal level of the first symbol in the second

codeword (i.e., $s_1^{(k+1)}$, wherein k = 1, 2, 3,...) from a logic

5   "01" signal level (e.g., represented by 1) to a logic "10"

signal level (e.g., represented by -3). These changes in the

logic states of the C_1 bit in the MSB codeword (M<4:0>) and the

C_2 bit in the LSB codeword (L<4:0>) may represent any number of

types of additional information, such as, for example, control

10   information, data information, error information, framing

information, synchronization information, etc..

Referring to Figure 7A, there is shown modified 4S5S

encoder circuitry 700A for use in utilizing spare bandwidth

resulting from the use of a 4S5S transition-limiting code, such

15   as described in the above-referenced U.S. Patent Application No.

10/314,985, in a 4-PAM signaling system, such as shown in Figure

3, for the Case I(a), Case II(a), and Case IV(a) scenarios

described above in Figures 4, 5, and 6, respectively, in

accordance with the present invention. The modified 4S5S

20   encoder circuitry 700A comprises a 4S5S encoder 702, delay

circuitry 704, logic function circuitry 706, an inverter circuit

708, a plurality of logic "AND" function circuits 710, and a

plurality of logic "OR" function circuits 712.

The 4S5S encoder 702 receives parallel input data $D_{in}<7:0>$, and then encodes the received parallel input data $D_{in}<7:0>$ so as to provide parallel codewords to a serializing 4-PAM transmitter (not shown) that are organized as MSB codewords ($M<4:0>$) and LSB

5 codewords ($L<4:0>$). As described above, the parallel input data $D_{in}<7:0>$ is received as an 8-bit word. The MSB codewords ($M<4:0>$) and the LSB codewords ($L<4:0>$) each have 5 bits, wherein each MSB codeword ($M<4:0>$) has five codeword bits organized as $<C_1, C_3, C_5, C_7, C_9>$ and each LSB codeword ($L<4:0>$)

10 has five codeword bits organized as $<C_2, C_4, C_6, C_8, C_{10}>$. Thus, the MSB codewords ($M<4:0>$) and the LSB codewords ($L<4:0>$) together form 10-bit codewords that are represented by groups of consecutive 2-bit symbols. The 4S5S encoder 702 may be implemented with binary logic.

15 All of the other circuitry in the modified 4S5S encoder circuitry 700A of Figure 7A operates to determine whether or not the C_2 bit in the LSB codeword ($L<4:0>$) may be changed from a logic "1" state to a logic "0" state so that spare bandwidth associated with periodically unused outer 4-PAM signal levels

20 may be used for other beneficial purposes in accordance with the present invention. That is, the delay circuitry 704 provides a 5T delay for both the C_9 bit in the MSB codeword ($M<4:0>$) and the C_{10} bit in the LSB codeword ($L<4:0>$), wherein T is the symbol

period as defined above. The logic function circuitry 706

operates according to the symbol domain and codeword bit domain

logic tables shown in Figures 4-6, and the m_1, m_2, and m_4 outputs

are defined by the functions shown in Figures 4-6. The logic

5 function circuitry 706 may be implemented with binary logic.

The inverter circuit 708 inverts the state of the C_1 bit in

the MSB codeword (M<4:0>) for use by one of the plurality of

logic "AND" function circuits 710. Outputs m_1, m_2, and m_4 from

the logic function circuitry and spare bandwidth input signals

10 (i.e., spare$_H$ and spare$_L$), which represent additional information

to be transmitted in spare bandwidth associated with

periodically unused outer 4-PAM signal levels, are applied to

the remaining plurality of logic "OR" function circuits 712 and

logic "AND" function circuits 710 so as to generate "Invert C_2"

15 and "Spare TX Ack" output signals. More specifically, the spare$_H$

signal represents additional information to be transmitted in

spare bandwidth associated with the uppermost signal level

(i.e., 00) of the first symbol in the second codeword (i.e.,

$s_1^{(k+1)}$, wherein k = 1, 2, 3,...), and the spare$_L$ signal represents

20 additional information to be transmitted in spare bandwidth

associated with the lowermost signal level (i.e., 10) of the

first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1,

2, 3,...). The "Invert C_2" signal is used to change the C_2 bit

in the LSB codeword (L<4:0>) from a logic "1" state to a logic

"0" state so that spare bandwidth associated with periodically

unused outer 4-PAM signal levels may be used for other

beneficial purposes in accordance with the present invention.

5   As described above, this change in the logic state of the C_2 bit

in the LSB codeword (L<4:0>) may represent any number of types

of additional information, such as, for example, control

information, data information, error information, framing

information, synchronization information, etc.. The "Spare TX

10   Ack" signal provides a notification to circuitry that generates

the $spare_H$ and $spare_L$ signals (not shown) that the additional

information represented by the $spare_H$ or $spare_L$ signals has

actually been transmitted. Referring to Figure 7B, there is

shown modified 4S5S encoder circuitry 700B for use in utilizing

15   spare bandwidth resulting from the use of a 4S5S transition-

limiting code, such as described in the above-referenced U.S.

Patent Application No. 10/314,985, in a 4-PAM signaling system,

such as shown in Figure 3, for the Case I(b), Case II(b), and

Case IV(b) scenarios described above in Figures 4, 5, and 6,

20   respectively, in accordance with the present invention. The

modified 4S5S encoder circuitry 700B of Figure B is similar to

the modified 4S5S encoder circuitry 700A of Figure 7A, except

that the inverter circuit 708 is connected differently so as to

allow for the generation of an additional "Invert C_1" signal for use in changing the logic state of the C_1 bit in the MSB codeword (M<4:0>).

5 Referring to Figure 8A, there is shown an alternative embodiment to the modified 4S5S encoder circuitry 700A of Figure 7A. That is, Figure 8A shows modified 4S5S encoder and serializing 4-PAM transmitter circuitry 800A for use in utilizing spare bandwidth resulting from the use of a 4S5S transition-limiting code, such as described in the above-

10 referenced U.S. Patent Application No. 10/314,985, in a 4-PAM signaling system, such as shown in Figure 3, for the Case I(a), Case II(a), and Case IV(a) scenarios described above in Figures 4, 5, and 6, respectively, in accordance with the present invention. The modified circuitry 800A comprises a modified

15 4S5S encoder 802, a modified serializing 4-PAM transmitter 804, a plurality of logic "OR" function circuits 808, an inverter circuit 810, and a plurality of logic "AND" function circuits 812.

The modified 4S5S encoder 802 receives parallel input data

20 D_{in}<7:0>, and then encodes the received parallel input data D_{in}<7:0> so as to provide parallel codewords to the modified serializing 4-PAM transmitter 804 that are organized as MSB codewords (M<4:0>) and LSB codewords (L<4:0>). As described

above, the parallel input data $D_{in}<7:0>$ is received as an 8-bit word. The MSB codewords ($M<4:0>$) and the LSB codewords ($L<4:0>$) each have 5 bits, wherein each MSB codeword ($M<4:0>$) has five codeword bits organized as $<C_1, C_3, C_5, C_7, C_9>$ and each LSB

5   codeword ($L<4:0>$) has five codeword bits organized as $<C_2, C_4, C_6, C_8, C_{10}>$. Thus, the MSB codewords ($M<4:0>$) and the LSB codewords ($L<4:0>$) together form 10-bit codewords that are represented by groups of consecutive 2-bit symbols.

The modified 4S5S encoder 802 is functionally equivalent to

10   the combination of the 4S5S encoder 702, the delay circuitry 704, and the logic function circuitry 706 of the modified 4S5S encoder circuitry 700A of Figure 7A. Thus, the modified 4S5S encoder 802 operates in a manner that is functionally equivalent to the above-described operation of the 4S5S encoder 702, the

15   delay circuitry 704, and the logic function circuitry 706 of the modified 4S5S encoder circuitry 700A of Figure 7A. The modified 4S5S encoder 802 may be implemented with binary logic.

The inverter circuit 810 inverts the state of the C_1 bit in the MSB codeword ($M<4:0>$) for use by one of the plurality of

20   logic "AND" function circuits 812. Outputs m_1, m_2, and m_4 from the modified 4S5S encoder 802 and spare bandwidth input signals (i.e., $spare_H$ and $spare_L$), which represent additional information to be transmitted in spare bandwidth associated with

periodically unused outer 4-PAM signal levels, are applied to

most of the remaining plurality of logic "OR" function circuits

808 and logic "AND" function circuits 812 so as to generate

"change$_H$" and "change$_L$" control signals for use by the modified

5   serializing 4-PAM transmitter 804. More specifically, the spare$_H$

control signal represents additional information to be

transmitted by the modified serializing 4-PAM transmitter 804 in

spare bandwidth associated with the uppermost signal level

(i.e., 00) of the first symbol in the second codeword (i.e.,

10   $s_1^{(k+1)}$, wherein k = 1, 2, 3,...), and the spare$_L$ control signal

represents additional information to be transmitted by the

modified serializing 4-PAM transmitter 804 in spare bandwidth

associated with the lowermost signal level (i.e., 10) of the

first symbol in the second codeword (i.e., $s_1^{(k+1)}$, wherein k = 1,

15   2, 3,...). The modified serializing 4-PAM transmitter 804

comprises a differential transmitter 806 for differentially

serially transmitting the parallel codewords received from the

modified 4S5S encoder 802 based upon the logic states of the

change$_H$ and change$_L$ control signals. That is, based upon the

20   logic states of the change$_H$ and change$_L$ control signals, the

modified serializing 4-PAM transmitter 804 may change the signal

levels of the serial data formed from the MSB codewords (M<4:0>)

and the LSB codewords (L<4:0>) received from the modified 4S5S

encoder 802 so that spare bandwidth associated with periodically

unused outer 4-PAM signal levels may be used for other

beneficial purposes in accordance with the present invention.

In the embodiment of Figure 8A, the control signals (i.e.,

5    $change_H$ and $change_L$) are used to change the logic state of the C_2

bit in the LSB codeword (L<4:0>). More specifically, in the

embodiment of Figure 8A, when the $change_H$ or $change_L$ control

signal is activated, the modified serializing 4-PAM transmitter

804 changes the signal level of the first symbol of the code

10   word (i.e., M<4:0> and L<4:0>, where M<4:0> comprises C_1, C_3, C_5,

C_7 C_9 and where L<4:0> comprises C_2, C_4, C_6, C_8 C_{10}) from an inner

signal level to a corresponding outer signal level. When the

$change_H$ control signal is activated, the signal level of the

first symbol of the code word from Modified 4S5S Encoder 802 is

15   at a logic signal level "01" (e.g., represented by +1), and the

modified serializing 4_PAM transmitter 804 changes the signal

level of this symbol to "00" (e.g., represented by +3). When

the $change_L$ control signal is activated, the signal level of the

first symbol of the code word from Modified 4S5S Encoder 802 is

20   at a logic signal level "11" (represented by -1), and the

modified serializing 4_PAM transmitter 804 changes the signal

level of this symbol to "10" (e.g., represented by -3).

As described above, this change in the signal levels of the

serial data formed from the MSB codewords (M<4:0>) and the LSB

codewords (L<4:0>) received from the modified 4S5S encoder 802

may represent any number of types of additional information,

such as, for example, control information, data information,

5   error information, framing information, synchronization

information, etc..

The $change_H$ and $change_L$ control signals are also applied to

a final remaining one of the plurality of logic "OR" function

circuits 808 so as to generate a "Spare TX Ack" signal, which

10   provides a notification to circuitry that generates the $spare_H$

and $spare_L$ control signals (not shown) that the additional

information represented by the $spare_H$ or $spare_L$ control signals

has actually been transmitted by the modified serializing 4-PAM

transmitter 804.

15   Referring to Figure 8B, there is shown an alternative

embodiment to the modified 4S5S encoder circuitry 700B of Figure

7B. That is, Figure 8B shows modified 4S5S encoder and

serializing 4-PAM transmitter circuitry 800B for use in

utilizing spare bandwidth resulting from the use of a 4S5S

20   transition-limiting code, such as described in the above-

referenced U.S. Patent Application No. 10/314,985, in a 4-PAM

signaling system, such as shown in Figure 3, for the Case I(b),

Case II(b), and Case IV(b) scenarios described above in Figures

4, 5, and 6, respectively, in accordance with the present

invention. The modified circuitry 800B of Figure 8B is similar

to the modified circuitry 800A of Figure 8A, except that the

control signals (i.e., change$_H$ and change$_L$ control signals) are

5   now used to change the logic states of both the C_1 bit in the MSB

codeword (M<4:0>) and the C_2 bit in the LSB codeword (L<4:0>).

In Figure 8B, the inverter circuit 810 is connected differently

than it is connected in Figure 8A. In Figure 8B, inverter

circuit 810 is connected so that it inverts the state of the C_1

10   bit in the MSB codeword (M<4:0>) for use by another one of the

plurality of logic "AND" function circuits 812. In Figure 8B,

when the change$_H$ or change$_L$ control signal is activated, the

modified serializing 4_PAM transmitter 804 changes the signal

level of the first symbol of the code word from an inner signal

15   level to an outer signal level. When the change$_H$ control signal

is activated, the signal level of the first symbol of the code

word from Modified 4S5S Encoder 802 is at logic signal level

"11" (e.g., represented by -1), and the modified serializing

4_PAM transmitter 804 changes the signal level of this symbol to

20   "00" (e.g., represented by +3). When the change$_L$ control signal

is activated, the signal level of the first symbol of the code

word from Modified 4S5S Encoder 802 is at logic signal level

"01" (e.g., represented by +1), and the modified serializing

4_PAM transmitter 804 changes the signal level of this symbol to

"10" (e.g., represented by -3).

Referring to Figure 9A, there is shown circuitry 900A for

use in receiving and decoding codewords that have been modified

5   to utilize spare bandwidth resulting from the use of a 4S5S

transition-limiting code, such as described in the above-

referenced U.S. Patent Application No. 10/314,985, in a 4-PAM

signaling system, such as shown in Figure 3, for the Case I(a),

Case II(a), and Case IV(a) scenarios described above in Figures

10   4, 5, and 6, respectively, in accordance with the present

invention. The circuitry 900A comprises a deserializing 4-PAM

receiver 902 and a modified 4S5S decoder 904A. The

deserializing 4-PAM receiver 902 comprises a differential

receiver 906 for differentially serially receiving the multiple

15   consecutive symbols in the MSB codewords (M<4:0>) and the LSB

codewords (L<4:0>) from a serializing 4-PAM transmitter (not

shown). The differential receiver 906 then transmits the MSB

codewords (M<4:0>) and the LSB codewords (L<4:0>) in parallel

form to the modified 4S5S decoder 904A.

20   The modified 4S5S decoder 904A comprises a plurality of

inverter circuits 908, a plurality of logic "AND" function

circuits 912, and a 4S5S decoder 914. The modified 4S5S decoder

904A receives the MSB codewords (M<4:0>) and the LSB codewords

(L<4:0>) in parallel form from the differential receiver 906. A

first of the plurality of inverter circuits 908 inverts the

state of the C_1 bit in the received MSB codeword (M<4:0>) for use

by one of the plurality of logic "AND" function circuits 912. A

5   second of the plurality of inverter circuits 908 inverts the

state of the C_2 bit in the received LSB codeword (L<4:0>) for use

by both the plurality of logic "AND" function circuits 912. The

plurality of logic "AND" function circuits 912 receive the

inverted and non-inverted C_1 bit and the inverted C_2 bit, and

10   generate output signals (i.e., $spare_H$ and $spare_L$ signals)

indicating if the received codeword contains additional

information in the spare bandwidth associated with periodically

unused outer 4-PAM signal levels in accordance with the present

invention. As described above, this additional information may

15   comprise, for example, control information, data information,

error information, framing information, synchronization

information, etc..

A "Set C_2 = 1" signal is used to change the C_2 bit in the

LSB codeword (L<4:0>) from a logic "0" state to a logic "1"

20   state so as to return the LSB codeword (L<4:0>) to its original

unmodified state.

The 4S5S decoder 914 receives the MSB codewords (M<4:0>)

and the updated LSB codewords (L<4:0>) in parallel form, and

then decodes the received MSB codewords ($M<4:0>$) and the

received LSB codewords ($L<4:0>$) so as to provide parallel output

data $D_{out}<7:0>$. The parallel output data $D_{out}<7:0>$ is provided as

an 8-bit word. The 4S5S decoder 914 may be implemented with

5 binary logic.

Referring to Figure 9B, there is shown circuitry 900B for

use in receiving and decoding codewords that have been modified

to utilize spare bandwidth resulting from the use of a 4S5S

transition-limiting code, such as described in the above-

10 referenced U.S. Patent Application No. 10/314,985, in a 4-PAM

signaling system, such as shown in Figure 3, for the Case I(b),

Case II(b), and Case IV(b) scenarios described above in Figures

4, 5, and 6, respectively, in accordance with the present

invention. The circuitry 900B of Figure 9B is similar to the

15 circuitry 900A of Figure 9A, except for the addition of an

"EXCLUSIVE-OR" logic function circuit 916 for generating a "C_1"

signal for use in changing the logic state of the C_1 bit in the

MSB codeword ($M<4:0>$) so as to return the MSB codeword ($M<4:0>$)

to its original unmodified state.

20 Referring to Figure 10A, there is shown an alternative

embodiment to the circuitry 900A of Figure 9A and the circuitry

900B of Figure 9B. That is, Figure 10A also shows circuitry

1000 for use in receiving and decoding codewords that have been

modified to utilize spare bandwidth resulting from the use of a

4S5S transition-limiting code, such as described in the above-

referenced U.S. Patent Application No. 10/314,985, in a 4-PAM

signaling system, such as shown in Figure 3, for the Case I(a),

5   Case II(a), and Case IV(a) scenarios described above in Figures

4, 5, and 6, respectively, in accordance with the present

invention. The circuitry 1000 comprises a modified

deserializing 4-PAM receiver 1002 and a 4S5S decoder 1004. The

modified deserializing 4-PAM receiver 1002 comprises a modified

10   detector 1006 and a differential receiver 1008. The modified

detector 1006 comprises a 4-PAM detector 1010 and an S_1 level

detector 1012. The 4-PAM detector 1010 detects signal levels in

multiple consecutive symbols in differentially serially

transmitted MSB codewords (M<4:0>) and LSB codewords (L<4:0>)

15   received from a serializing 4-PAM transmitter (not shown).

These detected signal levels are provided to the S_1 level

detector 1012, which specifically determines if the first symbol

(i.e., S_1) in every received codeword is at a logic "00" signal

level (e.g., represented by +3) or at a logic "10" signal level

20   (e.g., represented by -3). If the S_1 level detector 1012

determines that the first symbol (i.e., S_1) in a received

codeword is at a logic "00" signal level (e.g., represented by

+3), then the S_1 level detector 1012 generates an output signal

(i.e., $spare_H$) indicating that the received codeword contains

additional information in the spare bandwidth associated with

periodically unused outer 4-PAM signal levels in accordance with

the present invention. Also, if the S_1 level detector 1012

5   determines that the first symbol (i.e., S_1) in a received

codeword is at a logic "10" signal level (e.g., represented by -

3), then the S_1 level detector 1012 generates an output signal

(i.e., $spare_L$) indicating that the received codeword contains

additional information in the spare bandwidth associated with

10   periodically unused outer 4-PAM signal levels in accordance with

the present invention. As described above, this additional

information may comprise, for example, control information, data

information, error information, framing information,

synchronization information, etc..

15   The S_1 level detector 1012 also provides control signals

back to the 4-PAM detector 1010. In the embodiment of Figure

10A, the control signals (i.e., $change_H$ and $change_L$) are used to

change the logic state of the C_2 bit in the received LSB codeword

(L<4:0>) from a logic "0" state to a logic "1" state. More

20   specifically, if the S_1 level detector 1012 determines that the

first symbol (i.e., S_1) in a received codeword is at a logic "00"

signal level (e.g., represented by +3), then the S_1 level

detector 1012 generates a control signal (i.e., $change_L$) for the

4-PAM detector 1010, which causes the 4-PAM detector 1010 to change the signal level of the serial data received at the 4-PAM detector 1010 so as to return the LSB codeword (L<4:0>) contained in the received serial data to its original unmodified

5   state. In the circuitry 1000 depicted in Figure 10A, if the S_1 level detector 1012 determines that the first symbol (i.e., S_1) in a received codeword is at a logic "00" signal level (e.g., represented by +3), then the S_1 level detector 1012 generates a control signal (i.e., change$_L$) for the 4-PAM detector 1010, which

10 causes the 4-PAM detector 1010 to change the signal level of the serial data received at the 4-PAM detector 1010 so as change the S_1 level from "00" to "01" (which results in a return of the LSB codeword (L<4:0>) contained in the received serial data to its original unmodified state). If the S_1 level detector 1012

15 determines that S_1 in a received codeword is at a logic "10" signal level (e.g., represented by -3), then the S_1 level detector 1012 generates a control signal (i.e., change$_H$) for the 4-PAM detector 1010, which causes the 4-PAM detector 1010 to change the signal level of the serial data received at the 4-PAM

20 detector 1010 so as change the S_1 level from "10" to "11" (which results in a return of the LSB codeword contained in the received serial data to its original unmodified state).

In the embodiment of Figure 10B, the control signals (i.e.,

change$_H$ and change$_L$) are used to change the logic states of both

the C_1 bit in the received MSB codeword (M<4:0>) and the C_2 bit in

the received LSB codeword (L<4:0>). More specifically, in the

circuitry 1000 depicted in Figure 10B, if the S_1 level detector

5   1012 determines that the first symbol (i.e., S_1) in a received

codeword is at a logic "00" signal level (e.g., represented by

+3), then the S_1 level detector 1012 generates a control signal

(i.e., change$_L$) for the 4-PAM detector 1010, which causes the 4-

PAM detector 1010 to change the signal level of the serial data

10   received at the 4-PAM detector 1010 so as change the S_1 level

from "00" to "11" (which results in a return of the received MSB

codeword (M<4:0>)and the received LSB codeword (L<4:0>) to their

original unmodified states). If the S_1 level detector 1012

determines that S_1 in a received codeword is at a logic "10"

15   signal level (e.g., represented by -3), then the S_1 level

detector 1012 generates a control signal (i.e., change$_H$) for the

4-PAM detector 1010, which causes the 4-PAM detector 1010 to

change the signal level of the serial data received at the 4-PAM

detector 1010 so as change the S_1 level from "10" to "01" (which

20   results in a return of the received MSB codeword (M<4:0>) and

the received LSB codeword (L<4:0>) to their original unmodified

states).

The modified detector 1006 provides updated differential

serial codewords to the differential receiver 1008, which

operates similar to the differential receiver 906 in Figures 9A

and 9B. The differential receiver 1008 provides MSB codewords

(M<4:0>) and updated LSB codewords (L<4:0>) in parallel form to

5   the 4S5S decoder 1004, which operates similar to the 4S5S

decoder 914 in Figures 9A and 9B.

At this point it should be noted that transmission errors

may also be detected using a modified 4S5S decoder in accordance

with the present invention. More specifically, referring to

10   Figure 11, there are shown symbol domain and codeword bit domain

logic tables for determining when spare bandwidth associated

with periodically unused outer 4-PAM signal levels may be used

to detect transmission errors in accordance with the present

invention. That is, if the error detection conditions as

15   defined in Figure 11 are met, then an error is present in a

codeword.

Referring to Figure 12A, there is shown circuitry 1200A for

use in receiving and decoding codewords that may have been

modified to utilize spare bandwidth resulting from the use of a

20   4S5S transition-limiting code, such as described in the above-

referenced U.S. Patent Application No. 10/314,985, in a 4-PAM

signaling system, such as shown in Figure 3, for the Case I(a),

Case II(a), and Case IV(a) scenarios described above in Figures

4, 5, and 6, respectively, in accordance with the present

invention. The circuitry 1200A comprises a deserializing 4-PAM

receiver 902 and a modified 4S5S decoder 1202A. The

deserializing 4-PAM receiver 902 in Figure 12A operates similar

5   to the deserializing 4-PAM receiver 902 in Figure 9A, and thus

no further description is required. The modified 4S5S decoder

1202A operates similar to the modified 4S5S decoder 904A in

Figure 9A, except for additional error detection circuitry

comprising delay circuitry 1204 and logic function circuitry

10   1206. The delay circuitry 1204 provides a 5T delay for both the

C_9 bit in the MSB codeword (M<4:0>) and the C_{10} bit in the LSB

codeword (L<4:0>), wherein T is the symbol period as defined

above. The logic function circuitry 1206 operates according to

the symbol domain and codeword bit domain logic tables shown in

15   Figure 11. That is, when the error detection conditions as

defined in Figure 11 are met, then the logic function circuitry

1206 generates an error signal (i.e., Error Detected). The

logic function circuitry 1206 may be implemented with binary

logic.

20   Referring to Figure 12B, there is shown circuitry 1200B for

use in receiving and decoding codewords that may have been

modified to utilize spare bandwidth resulting from the use of a

4S5S transition-limiting code, such as described in the above-

referenced U.S. Patent Application No. 10/314,985, in a 4-PAM

signaling system, such as shown in Figure 3, for the Case I(b),

Case II(b), and Case IV(b) scenarios described above in Figures

4, 5, and 6, respectively, in accordance with the present

5   invention. The circuitry 1200B of Figure 12B is similar to the

circuitry 1200A of Figure 12A, except that the circuitry 1200B

of Figure 12B comprises a modified 4S5S decoder 1202B that

operates similar to the modified 4S5S decoder 904B in Figure 9B,

except for the additional error detection circuitry comprising

10   the delay circuitry 1204 and the logic function circuitry 1206.

At this point it should be noted that utilizing spare

bandwidth resulting from the use of transition-limiting codes in

multi-PAM signaling systems in accordance with the present

invention as described above may involve the processing of input

15   data and the generation of output data to some extent. This

input data processing and output data generation may be

implemented in hardware or software. For example, as described

above, specific electronic components may be employed in an

encoder, decoder, or other similar or related circuitry for

20   implementing the functions associated with utilizing spare

bandwidth resulting from the use of transition-limiting codes in

multi-PAM signaling systems in accordance with the present

invention as described above. Alternatively, one or more

processors operating in accordance with stored instructions may

implement the functions associated with utilizing spare

bandwidth resulting from the use of transition-limiting codes in

multi-PAM signaling systems in accordance with the present

5   invention as described above. If such is the case, it is within

the scope of the present invention that such instructions may be

stored on one or more processor readable carriers (e.g., a

magnetic disk), or transmitted to one or more processors via one

or more signals.

10   The present invention is not to be limited in scope by the

specific embodiments described herein. Indeed, other various

modifications of and modifications to the present invention, in

addition to those described herein, will be apparent to those of

ordinary skill in the art from the foregoing description and

15   accompanying drawings. Thus, such other embodiments and

modifications are intended to fall within the scope of the

following appended claims. Further, although the present

invention has been described herein in the context of a

particular implementation in a particular environment for a

20   particular purpose, those of ordinary skill in the art will

recognize that its usefulness is not limited thereto and that

the present invention can be beneficially implemented in any

number of environments for any number of purposes. Accordingly,

the claims set forth below should be construed in view of the

full breath and spirit of the present invention as disclosed

herein.